


IDS 7/15/05 1/2

PTO/SB/08A (07-05)

Approved for use through 07/31/2006. OMB 0661-0031
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Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/824,628
		Filing Date	07/21/2003
		First Named Inventor	Luan C. Tran
		Art Unit	2812
		Examiner Name	J. Kennedy
Sheet 1 of 2	Attorney Docket Number	MI22-2356	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,532,107	7/1996	Ole et al.	
		US- 2001/0006752	7/2001	Watanabe et al.	
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁵
		Country Code ²	Number * Kind Code ³ (if known)				
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Examiner Signature	<i>[Signature]</i>	Date Considered	Oct 28, 2005
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IDS 7/15 2/2

PTO/SB/088 (08-03)

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Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/624,628
		Filing Date	July 21, 2003
		First Named Inventor	Luan C. Tran
		Art Unit	2812
		Examiner Name	J. Kennedy
		Attorney Docket Number	MI22-2356
Sheet 2	of 2		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JM		Wolf et al., Silicon Processing for the VLSI Era, Volume 1-Process Technology, Second Edition, Lattice Press, 2000, pgs. 515-517.	
JM		Wolf et al., Silicon Processing for the VLSI Era, Volume 1-Process Technology, Second Edition, Lattice Press, 2000, pgs. 527-531.	

Examiner Signature	<i>Quinn M. Kennedy</i>	Date Considered	Oct 28, 2005
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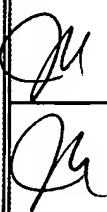
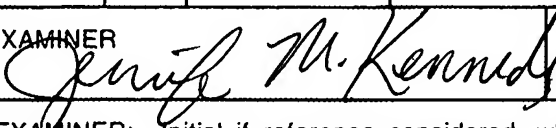
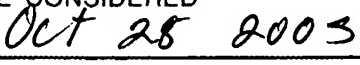
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Sheet 1 of 1

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2356		SERIAL NO. 10/624,628		
 PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran				
				FILING DATE July 21, 2003		GROUP 2812		
U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,970,352	10/99	Shiozawa et al.				
	AB	6,001,707	12/99	Lin et al.				
	AC	6,420,749	07/02	Divakaruni et al.				
	AD	6,187,624	02/01	Huang				
	AE	5,946,568	08/99	Hsiao et al.				
	AF	6,242,329	06/01	Huster et al.				
	AG	4,985,740	01/91	Shenai et al.				
	AH	US2002/0006693	01/02	Matsuda				
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AP							
	AQ							
	AR							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AS		Wolf et al., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Second Edition, Lattice Press 2000, pp.12-13, 25-27.					
	AT		S.M. Sze, VLSI Technology, Second Edition, McGraw-Hill, 1988, pages 472-483					
EXAMINER  DATE CONSIDERED 								
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								